IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR PATENT

LIGHT EMITTING SYSTEM WITH HIGH EXTRACTION EFFICIENCY

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Background of the Invention:

[0001] Rapid advances in solid state lighting systems such as high-brightness Light emitting diode (HB-LED) technology in the last decade have opened up the possibility of using LEDs as sources of general illumination in the not-too-distant future. Remarkable progress in LED efficiency, lifetime and total lumen output has enabled an early market in niche lighting applications such as traffic lights, brake lights, mobile phones, and outdoor signs. The rapid progress in LED technology has led to the belief that LED could have a significant impact on the lighting market within the next ten years. Illumination accounts directly for about 20 % of U.S. electricity consumption. With advanced LED technology, the energy consumption can be reduced significantly.

[0002] The key components of the luminous performance are the internal quantum efficiency and the extraction efficiency. Utilizing high quality material and advanced epitaxial growth technologies such as Molecular Beam Epitaxy (MBE) and Metal-Organic Chemical Vapor Deposition (MOCVD) to facilitate band gap engineering such as Multiple Quantum Wells (MQWs) structure, the internal quantum efficiency is approaching 100 %. In contrast, the extraction efficiency still needs much improvement. The extraction efficiency is the fraction of generated light that escapes from the semiconductor chip into the surrounding air or encapsulating epoxy, and is the fraction that is useful for illumination and other purposes. This is a challenging problem because the chip may have a much higher index of refraction, typically 3.4 for GaAs-based material, compared with 1.0 for air and approximately 1.5 for epoxy. This results in a critical angle of 17 degrees for air and 26 degrees for epoxy. If we consider a single

surface, the light can only escape if it strikes the surface within the critical angle. Therefore, the extraction efficiency out of a single surface is only 2.2 % into air and 4 % into epoxy. The rest of light is reflected from the surface back into the active layer and reabsorbed by the semiconductor material or reflected at other surfaces.

[0003] The extraction efficiency is one of the main themes for improving the energy efficiency of LED. Methods such as random surface texture, grating thin film (US 5,779,924), modifying chip geometry using, for example, truncated inverted pyramid (US 6,323,063) and photonic crystal structure (US5,955,749 & US2003/014150) are implemented. None of these approaches is entirely satisfactory. It is therefore desirable to provide an improved LED with better characteristics.

Summary of the Invention:

[0004] The present invention proposes a novel configuration for the solid state lighting systems to achieve extraction efficiency and optical emission from electrical pumping in the active layer superior to the above-mentioned conventional methods. The present invention can also be used to manipulate the majority of light emission to emerge vertically from the wafer surface.

[0005] In an epitaxial structure of a solid state Light Emitting system, electrical current injection into the active layer is used to excite the photon emission. The present invention employs one or more structures (such as layers) different from the active layer for trapping the light generated by the active layer. Then another structure is used for extracting the light trapped. In one embodiment, the light generated by the active layer is trapped by means of a unique waveguide layer in the epitaxial structure to achieve high performance. The waveguide layer preferably traps a significant portion of the radiation generated by the active layer in a single mode (e.g. its fundamental mode) or a few lower-order modes. This is a completely new feature in solid state lighting system design. Furthermore, one embodiment of the present invention employs multiple photonic crystal regions located either outside or inside one or more current injection regions to extract photons from the waveguide layer(s). This novel design optimizes the interplay of

electrical pumping, radiation and optical extraction to increase the optical output to several times that of conventional solid state lighting systems. In another embodiment, a transparent and conductive ITO layer is added to the surface of an epitaxial structure to reduce the interface reflection in addition to functioning as a current spreading layer. Each of the above-described features can be used separately or in conjunction with any one of the other features for improved performance. The present invention creates solid state lighting systems with high optical output and high power efficiency.

[0006] Thus, according to an embodiment of another aspect of the invention, the radiation generated by an active layer in a semiconductor structure in response to current injection is trapped, preferably in a single mode or a few lower-order modes, and the trapped radiation is extracted, preferably by means other than the means used to trap the radiation. In one embodiment, the trapping is performed by means of a waveguide layer which traps the radiation in its fundamental mode or a few lower-order modes. The extraction is preferably performed by means of photonic crystal structures.

[0007] In order to form the photonic crystal structures, which may be of nanometer dimensions, a layer of resist is formed on top of a semiconductor structure, and a pattern of indentations is formed on the resist layer by imprinting the pattern using a mold. A certain thickness of the resist layer is then removed, preferably by a process such as etching, to expose the surface of the semiconductor structure in a pattern that matches the pattern of indentations imprinted on the resist layer, while retaining a layer of resist that still covers the structure except for the pattern of exposed areas. A pattern of holes is then drilled, such as by etching, into the exposed areas of the semiconductor structure to form the photonic crystal structures. The making of the photonic crystal structures may be preferably performed after the semiconductor epitaxial structure is complete except for the formation of the photonic crystal structures and electrodes. The imprinting may be performed, in one embodiment, using a positive mold with protruding pillars, which preferably have cylindrical shapes. In one implementation, the mold may be made from replication from a negative mold made using electron beam lithography or Optical lithography.

Brief Description of the Drawings:

[0008] Fig. 1 is a cross-sectional view that shows an epitaxial structure having a waveguide structure and suitable for implementing a photonic crystal structure to illustrate an embodiment of the invention;

[0009] Fig. 2 is a cross-sectional view that shows that the holes are drilled through the epitaxial layers of the structure of Fig. 1 by a process such as chemical etching to improve light extraction;

[0010] Figs. 3A-3D show the arrangement of photonic crystal pattern and current electrodes from the wafer level to the individual hole for LEDs to illustrate an embodiment of the invention;

[0011] Fig. 4A is a cross-sectional view that shows one embodiment with electrode region overlapping a part of photonic crystal region;

[0012] Fig. 4B is a cross-sectional view that shows another embodiment with the current injection regions substantially segregated from the photonic crystal regions;

[0013] Fig. 5 shows an example of hexagonal PC cells arranged in a chip for LEDs;

[0014] Fig. 6 shows the triangular array of holes fits into a hexagonal cell for LEDs;

[0015] Fig. 7 illustrates a nano-imprint process used to create a photonic crystal pattern on a wafer, starting with the structure in Fig. 1.

Detailed Description of the Invention:

[0016] In order to illustrate one embodiment of the present invention directed to a solid state lighting system having a photonic crystal (PC) structure with clarity, we first present an epitaxial structure suitable for implementing photonic crystal and then add the photonic crystal structure into the epitaxial structure. Figure 1 shows the epitaxial structure of the present invention without the PC structure. All epitaxial layers are grown on the top of the substrate 110. The substrate material is typically GaAs for red or yellow light emission structures and Sapphire, GaN or SiC for UV, blue and green light emission structures. Layer 121 is the active layer, where holes and electrons combine to emit light. The epitaxial structure of active layer 121 can be double heterostructure, multi-quantum wells (MQWs), or multi-quantum dots (MQDs) to optimize the internal quantum efficiency.

[0017] Holes and electrons combine in the active layer 121, causing light to be spontaneously generated from the layer. Then a large portion of emitted photons from the active layer 121 is trapped within the waveguide layers 122 and 123 as well as the active layer 121. Active layer 121 cannot serve as a waveguide core layer because usually it is very thin. In the present invention we arrange one or two additional waveguide layers with the refractive index close to that of the active layer and with the appropriate thickness. The index of refraction of the waveguide layers 122 and 123 is higher than that of the cladding layers 124 and 131, whose thickness(es) is more than 50 nm. The un-trapped light exits the semiconductor surfaces or is re-absorbed by the semiconductor structure in the same manner as in conventional LEDs. The waveguide layers, 122 and 123, are designed to allow the optical power to travel along the waveguide in one single mode or a few lower-order modes. To achieve such result, the thickness(es) of each of waveguide layers 122 and 123 is about 30 nm to 250 nm. Extraction by Photonic Crystal will not be effective if the waveguide supports a number of modes with quite different propagation constants because the band edge of PC structure may correspond to only one mode or a few modes. Prior LED epitaxial structures, such as the ones in Patent Application US 2003/0141507, do not contain any waveguide layer like the ones in embodiments of the present invention.

[0018] Layer 124 in Fig 1 is a contact layer to provide a transition to an ultra thin metal layer 125, which is followed by an Indium Tin Oxide (ITO) layer 126. ITO layer 126 and Ultra thin metal layer 125 are used to increase current spreading over the wafer surface. Current spreading layers for LEDs are described in U.S. patent application, Ser. No. 10/641,641, filed Aug. 14, 2003, which application is incorporated by reference herein in its entirety. The ITO is transparent and conductive and its index of refraction is about 1.8. It also acts as an antireflection coating to reduce the Fresnel reflection at the air interface or the interface to external media such as encapsulating epoxy. Generally the Fresnel reflection at semiconductor epitaxial-air interface is high due to high index of semiconductor materials, which results in about 17 % reflection at GaN-based material-air interface and 30 % reflection at GaAs-based material-air interface. Therefore the ITO layer 126 plays a significant role on enhancing the optical output. Other conductive and transparent material, which has index of refraction lower than those of semiconductor layers, can be used to replace ITO as the material used for the current spreading layer which also reduces Fresnel reflection.

[0019] For minimizing reflection from the interface with air or other media, the thickness of ITO layer 126 is preferably equal to $\lambda/ (4 n_{ito})$, where λ is wavelength and n_{ito} is the index of refraction of the ITO. The thickness of the ITO layer is about 89 nm for 640 nm optical emission and 65 nm for 470 nm optical emission. The thickness of ITO can range from 30 nm to 300 nm to cover emission from ultra-UV to near infrared. For some cases in the present invention, the ITO layer 126 and the ultra-thin metal layer 125 can be omitted without adversely affecting the extraction, but with lower optical output due to high reflection at the epitaxy-air interface. After the wafer epitaxial growth and/or the photonic crystal structure have been completed or formed, metal electrode 127 is deposited. The injection current from the electrode 127 flows through the active layer to electrically pump it to radiate. To reduce the loss of optical power through the substrate 110, a Distributed Bragg Reflector (DBR) layer 133 can be implemented to reflect the photons upward towards electrode 127. This layer 133 can be omitted without affecting the emission function of the solid state light emitting system. Buffer layer 132 is to provide a transition from the cladding layer 131 to the DBR layer 133. In view of the

carrier transport in semiconductors, all semiconductor layers above the active layer 121 as shown in Fig. 1 can be either N-type or P type. The type of the semiconductor layers beneath the active layer 121 should be complementary to that above the active layer.

[0020] Fig. 2 and Fig. 3 show how a light extraction structure can be implemented in conjunction with the waveguide structure for improved performance. In one embodiment, this light extraction structure comprises a photonic crystal structure. This structure of one embodiment of the present invention is created, starting with the structure in Fig. 1, for improved light extraction. The photonic crystal structure comprises many holes through some of the layers drilled into the epitaxial structure of the solid state light emitting system in Fig. 1, where the holes preferably form a two-dimensional pattern. The present invention illustrates novel patterns for optimizing light extraction. In one embodiment, the electrode region superposes a part of the photonic crystal region as shown in Fig. 4A. The injection current supplied from the electrode and current source (connection between the source and the electrodes not shown) is intended to spread out through the ITO layer over the full PC region as shown in Fig. 4A. In another embodiment, the optical extraction region where the PC is located is substantially separated from the current injection region as shown in Fig. 4B. Holes 201 in Fig 2 are preferably created by chemical etching. The hole etching or drilling can be stopped at cladding layer 124 or waveguide layer 122 or the drilling or etching can even punch holes through the active layer 121 and waveguide layer 123 as indicated by dotted line 203. The hole diameter is in the range of 50nm to 300 nm (nano-meters) for visible light. The lattice constant a of the PC, the distance from the center of a hole to the center of the adjacent hole in the lattice of the PC, is from 80 nm to 500 nm for visible light. The lattice constant generally increases with the emitting wavelength and with the band number of the PC structure . The electrical field extending from the active layer 121 to the cladding layer 124, which is induced by the collective photons produced in the active layer 121, strongly interacts with the PC structure. At certain values for parameters of PC structure such as lattice constant and hole diameter as indicated below, the PC structure inhibits the photons from residing in the waveguide but emit vertically out of the wafer surface as indicated by 215 in Fig. 2.

[0021] Fig. 2 shows that the holes 201 are drilled from the top of the wafer. But when the wafer bonding technique is used, the holes can be imbedded from layers 131 or 123 or even through the active layer 121 into waveguide layer 122 and cladding layer 124. Wafer bonding technique is to flip over the epitaxial structure by taking out the original substrate such as 110 and then bond a new substrate on the original top layer such as the layer 124 if the ITO layer 126 in Fig. 2 is omitted. If the new substrate has a band gap that is wider than that of the active layer, the photons emitted by the active layer will not be significantly absorbed by the new substrate, so that light can be emitted from both sides of the solid state light emitting system. This may be advantageous for some applications. For example, where GaAs is the material in the original substrate for the solid state light emitting system, a material with a band gap that is wider than that of GaAs may be used, such as GaP.

[0022] Figs. 3A-3D are schematic views showing the arrangements of photonic crystal pattern and current electrodes from the wafer level to the individual hole that can be used in the solid state light emitting system of Figs. 1, 2, 4A and 4B. In lighting applications, the wafer 300 in Fig. 3A is broken into many chips 310, one of which is shown as indicated by the blow-up view of Fig. 3B. Each chip 310 has a side with length in the range of 50 to 500 μm. Within each chip 310, an electrode network 312 run across the chip surface vertically and horizontally to spread current more evenly. Each of the networks 312 may have a grid-shaped pattern as shown in Fig. 3B, where the pattern is formed by interconnected vertical and horizontal electrically conductive strips. Each of the network 312 therefore comprises a plurality of grid cells 316, each grid cell formed by two vertical strip segments and two horizontal elongated strip segments of the electrically conductive strips, where the segments are interconnected at their corners to form square or rectangular grid cells. Each grid cell 316 encloses a corresponding PC cell. The width d (see Fig. 3C) of the electrode strips in electrode networks 312 is about 1 to 100 μm. Each of the Photonic Crystal (PC) cells 315 is enclosed by a corresponding one of the grid cells in each of the electrode networks 312. Therefore there are many photonic crystal cells 315 in each chip. The size of each PC cell ranges from 1 to 100 μm on each side. The holes in a triangular array as indicated by 321 are created inside the PC

cell and beneath the electrodes as shown in Fig. 4A. Other hole arrays such as square or rectangular grid is also usable. The ITO layer 126 is used to spread the injection current supplied by the electrode over the full photonic crystal region. Therefore the current injection region, i.e. emitting region, overlaps the photonic crystal region, i.e. light extraction region.

[0023] To simplify the figures, the configuration for the current electrodes as illustrated in Figs. 3A-3D (and in Figs. 5 and 6 described below) are not shown in some of the remaining figures of this application, it being understood that the electrodes in such remaining figures (e.g. Fig. 4B) may take the shape in Figs. 3A-3D, 5, 6 or still other shapes.

[0024] In another embodiment, there is no hole beneath the electrode as shown in Fig. 4B. Current is injected by means of a current source (connection between the source and the electrodes not shown). The ITO layer 126 and ultra-thin metal layer 125 in Fig. 1 can be either kept or omitted for this case (the ITO layer is removed from Fig. 4B). Therefore the current injected primarily runs from the electrode 312 through the active layer 121 to the second electrodes 322 near the substrate, without passing through the portion of the epitaxial structure of the solid state light emitting system where the photonic crystal region is located. The photonic crystal region, which has holes, may have higher electrical resistance such that it is preferable to pass the current along paths away from this region. In this embodiment, the current injection region is substantially segregated from the photonic crystal region, which functions to extract light from the waveguide. One of advantages of this embodiment is to avoid the carrier (holes or electrons) loss in the photonic crystal region due to the defect and depletion on and near hole surfaces. The width of the electrode strips in network 312 (see Fig. 3C) is also optimized to have sufficient photons emitted in the active region underneath but having sufficient separation between the strips to allow the photons to travel between the electrode strips to reach the PC cell to emerge from the solid state light emitting system to be used for various purposes (such as illumination) without being significantly reabsorbed. The other advantage of this embodiment is that it allows the current injected

into the chip to be at elevated current density without overheating the semiconductor layers.

[0025] Inside the chip, the geometrical shapes of photonic crystal cells and electrodes can be arranged in many ways for the sake of optimizing optical and electrical performance of the solid state light emitting chip. Fig. 5 shows an example of hexagonal PC cells arranged in a chip. The hexagonal shape allows the photonic crystal to interact photons from all directions more effectively. Hexagonal cells are surrounded by electrode network 520 (white area in Fig. 5). As in the case of Figs. 3A-3D, since the hexagonal-shaped openings in the electrode (each opening in the electrode exposing a corresponding hexagonal PC cell) are arranged in a periodic array, arrays of network cells 316' of the electrode that are substantially similar to one another can be defined for the electrode in Fig. 5 as well. The term "network cell" therefore can be defined to encompass both the grid cells 316 of Figs. 3A-3D and those (316') of Fig. 5. The wire connected to the electrical power source can be bonded at 510 or at the edge 511. According to the theoretical calculation for the optimal performance for the case of no holes beneath the electrode 520, the electrode width W between two adjacent hexagonal cells is preferably approximately equal to $\sqrt{3}$ a, where a is the length of a side of the hexagon. Fig. 6 shows the triangular array of holes fitting into a hexagonal PC cell. Other shape arrangements are feasible and within the scope of the present invention.

[0026] The lattice constant and hole diameter of photonic crystal structure in the low order bands for visible light and UV are of the order of 100 nanometers. To create the PC arrays is a challenging task. At low throughput, electron beam lithography can be used to write the PC pattern, but is very slow. In the present invention, nano-imprint technology is introduced to create the PC pattern in mass production scale prior to the drilling of the holes by chemical etching. The main technique of nano-imprint consists of three basic components: a stamp with suitable feature sizes, a material such as photoresist or UV epoxy to be printed and equipment for printing with adequate control of printing conditions such as temperature and pressure.

[0027] Fig. 7 illustrates the nano-imprint process and its associated etching. As indicated above, the PC cells comprise holes of very small dimensions, which holes can be formed using the nano-imprint process of Fig. 7. The mold for making the nano-imprint in the Step 1 can be made by either electron beam lithography or Optical lithography. In the present invention, electron beam lithography is preferably used to make a mold with protruded nano-scale cylindrical pillars (positive mold) or nano-scale recessive holes (negative mold). Negative mold is used to replicate positive daughter molds for printing. For example, electron beam lithography or Optical lithography may be used to first make a negative mold, which is used in turn to replicate positive daughter molds that are actually used for the printing process.

[0028] A layer of resist is applied to the structure in Fig. 1 with the substrate 110 as support, since the surface layers of the structure in Fig. 1 may not be soft enough for making the nano-imprint. The material of the resist is typically a polymer such as PMMA and UV-cured epoxy. In step 2, the mold is pressed onto the resist layer, and then removed, to leave a pattern of indentations in the resist layer. In the steps 3 and 4, the etching can be carried out by ion-assisted chemical etching, reactive ion etching (RIE), induced coupled plasma (ICP) etching, physical sputtering and other methods. The etching is done to remove a certain thickness of the resist from the structure in Fig. 1. Since the pattern of indentations in the resist layer causes the resist to have a smaller thickness at the indentations, removal of a sufficient thickness of the resist from the substrate will expose regions of the structure in Fig. 1 where the pattern of indentations is located, while leaving the remainder of the resist to shield the rest of the structure surface. Therefore, the etching in steps 3 and 4 will result in holes being etched into the structure in Fig. 1 to form the solid state light emitting systems of Figs. 2, 4A and 4B.

[0029] While the invention has been described above by reference to various embodiments, it will be understood that changes and modifications may be made without departing from the scope of the invention, which is to be defined only by the appended claims and their equivalents. All references referred to herein are incorporated by reference herein in their entireties.